CBCS SCHEME

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15EC32

Third Semester B.E. Degree Examination, Jan./Feb.2021
Analog Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. With necessary equivalent diagram obtain the expression for Z_{in}, A_V, Z_0 for Darlington Emitter follower. **(10 Marks)**

b. For an Emitter bias circuit (capacitor bypassed), determine r_e, Z_i, Z_O and A_V. Given $R_B = 470\ K\Omega$, $R_C = 2.2\ K\Omega$, $V_{CC} = 20\ V$, $R_E = 0.56\ K\Omega$, $C_E = 10\ \mu F$, $\beta = 120$, $r_0 = 40\ K\Omega$, $C_C = 10\ \mu F$. **(06 Marks)**

OR

2 a. Derive the expression for A_V, A_i, Z_i and Z_0 for C_E fixed bias configuration using complete hybrid equivalent model. **(10 Marks)**

b. Consider a single stage CE amplifier with $R_S = 1\ K$ and $R_L = 1.2\ K\Omega$. Calculate A_i, R_i, A_V, A_{is}, if $h_{ie} = 1.1\ K$, $h_{re} = 2.5\times10^{-4}$, $h_{fe} = 50$ and $h_{oe} = 25\ \mu A/V$. **(06 Marks)**

Module-2

3 a. Derive the expression for transconductance g_m for FET. **(06 Marks)**

b. For the circuit shown in the Fig. Q3 (b), calculate (a) V_{GS} (b) I_{DQ} (c) V_{DSQ} (d) V_D. **(10 Marks)**

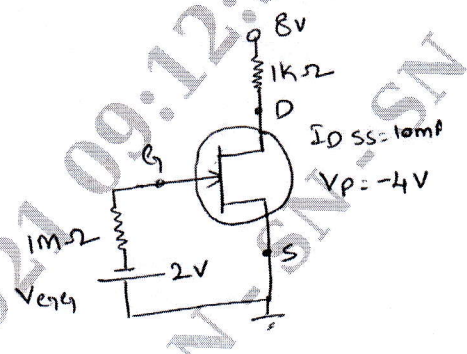

Fig. Q3 (b)

OR

4 a. With necessary equivalent circuit obtain the expression for A_V, Z_{in}, Z_O for a fixed biased JFET amplifier. **(08 Marks)**

b. Derive the expression for Z_i, Z_0, A_V considering common drain amplifier circuit. **(08 Marks)**

Module-3

5 a. Derive the expression for lower cut-of frequencies due to various RC networks in CE amplifiers. **(10 Marks)**

b. Determine the lower cut-off frequency for the emitter follower using BJT amplifier with $C_S = 0.1\ \mu F$, $R_S = 1\ K\Omega$, $R_1 = 12\ K\Omega$, $R_2 = 4\ K\Omega$, $R_E = 1.5\ K\Omega$, $C_C = 0.1\ \mu F$, $\beta = 100$, $r_0 = \infty$, $V_{CC} = 15\ V$, $V_{BE} = 0.7\ V$. **(06 Marks)**

OR

6 a. Describe Miller effect and derive an equation for Miller input and output capacitance. **(08 Marks)**

b. Calculate the overall lower 3 dB and upper 3 dB frequencies for a 3 stage amplifier having an individual $f_1 = 40$ Hz and $f_2 = 2$ MHz. **(08 Marks)**

Module-4

7 a. Derive the expression for input resistance for a voltage of series and current series feedback. **(08 Marks)**

b. With a neat circuit diagram, explain FET based phase shift oscillator. **(08 Marks)**

OR

8 a. With the help of neat circuit diagram. Explain the operation of Colpitts and Hartley oscillator. Write the expression for the frequency of oscillation. **(12 Marks)**

b. In a transistor Colpitts oscillator $C_1 = 1$ nF, $C_2 = 100$ nF. Find the value of L for a frequency of 100 kHz. **(04 Marks)**

Module-5

9 a. Show that the transformer coupled class A power amplifier has maximum efficiency of 50%. **(08 Marks)**

b. A single transistor amplifier with transformer coupled load produces harmonic amplitudes in the output as,
$B_0 = 1.5$ mA, $B_1 = 120$ mA, $B_2 = 10$ mA, $B_3 = 4$ mA, $B_4 = 2$ mA, $B_5 = 1$ mA
(i) Determine the percentage total harmonic distortion.
(ii) Assume a second identical transistor is used along with a suitable transformer to provide push pull operation. Use the above harmonic amplitudes to determine the new total harmonic distortion. **(08 Marks)**

OR

10 a. Explain with the block diagram, the basic types of voltage regulation circuit. **(08 Marks)**

b. Explain the operation of complementary symmetry class B amplifier. **(08 Marks)**

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